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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,320	09/29/2003	Robert M. Ellis	42P17514	4655

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EXAMINER	
SCHNEIDER, JOSHUA D	
ART UNIT	**PAPER NUMBER**
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,320	ELLIS ET AL.	
	Examiner	Art Unit	
	Joshua D. Schneider	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,10-12,27 and 39-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10-12,27 and 39-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/1/2007 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 27, 40, and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,845,472 to Walker et al.

5. With regards to claim 27, Walker teaches a processor (column 3, lines 25-35), a disk storage device coupled to the processor a memory controller coupled to the processor (column 3, lines 36-57), a first memory bus coupled to the memory controller (column 3, line 63, through column 4, line 11), a first memory device having a first storage array comprised of a plurality of

memory cells and a first interface buffer coupled within the first memory device to the first storage array (column 4, lines 27-45), first and second memory error logics associated with the interface buffer to carry out a check for memory errors within the storage array during an idle period associated with transactions carried out by the external memory controller on the first memory bus that involve the storage array (column 8, lines 46-51) and error checking is carried out in response to a read command from the memory controller (column 2, lines 9-46, and Claim 39).

6. With regards to claim 40, Walker teaches during the idle period, there are no transactions carried out by the memory controller on the first memory bus that involve the first storage array (column 8, lines 46-51).

7. With regards to claim 41, Walker teaches the first memory device further comprises a first bus error logic (Fig. 6, element 62) associated with the first interface buffer (Fig. 6, element 76) to carry out a check for bus errors in transactions across the first memory bus between the memory controller and the first interface (column 7, lines 45-57).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-4, 10-12, 39, and 46-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2004/0260991 to Vogt et al. in further view of U.S. Patent 6,349,390 to Dell et al. and U.S. Patent 6,845,472 to Walker et al.

10. With regards to claim 1, Vogt teaches a storage array comprised of a plurality of memory cells (Fig. 6, element 58); an interface buffer coupled to the storage array (Fig. 6, element 64), and having a first interface to couple the memory device to the a first memory bus to couple the memory device to a memory controller (Fig. 6, elements 54a/b and 56a/b); and memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array (paragraph 83). Vogt does not teach the error checking is carried out in response to a read command from the memory controller and during a an idle period associated with transactions carried out by the memory controller on the first memory bus that involve the storage array. Dell teaches a memory device with and memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array (Fig. 1, elements 10, 34, 62) and during a an idle period associated with transactions carried out by the memory controller on the first memory bus that involve the storage array (column 2, lines 8-35, and column 3, lines 23-64). It would have been obvious to one of ordinary skill in the art at the time of the invention to idle error correction system of Dell with the memory buffering error correction units Vogt of in order to decrease the number of errors without lowering system efficiency. Walker teaches a memory device with and memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array (Fig. 6, column 1, line 63, through column 2, line 8) and error checking is carried out in response to a read command from the memory controller (column 2, lines 9-46, and Claim 39). It would have been obvious to one of ordinary skill in the art at the time of the invention to read time error correction system of Walker with the memory buffering error correction units Vogt of in order to decrease the number of errors in system utilized data.

11. With regards to claim 2, Vogt teaches the memory error logic is a component of the interface buffer (paragraph 83), and wherein the memory device is comprised of a circuit board to which is attached at least one integrated circuit that comprises the storage array and at least one integrated circuit that comprises the interface buffer (Fig. 6, element 52).

12. With regards to claim 3, Vogt teaches the first memory bus provides a point-to-point connection between the memory device and the memory controller (Fig. 6, elements 50 and 52 connected by element 54), the interface buffer has a second interface to couple the memory device to the a second memory bus to provide a point-to-point connection between the memory device and another memory device (Fig. 6, elements 52 and second element 52 connected by second element 54), and the interface buffer passes through bus activity between the first and second memory busses that does not involve the storage array (paragraphs 39 and 42).

13. With regards to claim 4, Vogt teaches a transfer of data between the memory controller and the first interface of the interface buffer and a transfer of data between the second interface of the interface buffer and the another memory device occur with data transmitted in a packets (paragraph 42).

14. With regards to claim 10, Vogt fails to teach, but Dell teaches the memory error logic corrects a memory error, if a memory error is detected and is correctable, and the memory error logic transmits a signal to the memory controller if a memory error is detected and is not correctable (column 5, lines 24-58, and column 6, line 22-40). It would have been obvious to one of ordinary skill in the art at the time of the invention to error correction notification of Dell with the memory buffering error correction units Vogt of in order to decrease the number of read errors.

15. With regards to claim 11, Vogt fails to teach, Dell teaches bus error logic associated with the interface buffer to carry out a check for bus errors in transactions across the first memory bus between the external memory controller and the first interface (column 3, lines 23-64). It would have been obvious to one of ordinary skill in the art at the time of the invention to bus error checking of Dell with the memory buffering error correction units Vogt of in order to decrease the number of read errors.

16. With regards to claim 12, Vogt teaches a transaction across the first memory bus entails the transmission of data in a packet with CRC information, and the bus error logic examines the data and the CRC information to check for an occurrence of a bus error (paragraph 83).

17. With regards to claim 39, Vogt fails to teach, but Dell teaches wherein during the idle period, there are no transactions carried out by the memory controller on the first memory bus that involve the storage array (column 2, lines 8-35, and column 3, lines 23-64). It would have been obvious to one of ordinary skill in the art at the time of the invention to idle error correction system of Dell with the memory buffering error correction units Vogt of in order to decrease the number of errors without lowering system efficiency.

18. With regards to claim 46, Vogt teaches receiving a read command from a memory controller across a memory bus coupling the memory controller to a memory device (paragraphs 1 and 4); retrieving a check bit from a storage array of the memory device, in response to the read command (CRC bits, paragraph 83); and utilizing the check bit to check memory errors within the storage array, by a memory error logic of the memory device (CRC checking, paragraph 83). Vogt does not teach the error checking is carried out in response to a read command from the memory controller and during a an idle period associated with transactions

carried out by the memory controller on the first memory bus that involve the storage array. Dell teaches a memory device with and memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array (Fig. 1, elements 10, 34, 62) and during a an idle period associated with transactions carried out by the memory controller on the first memory bus that involve the storage array (column 2, lines 8-35, and column 3, lines 23-64). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the idle error correction system of Dell with the memory buffering error correction units Vogt of in order to decrease the number of errors without lowering system efficiency.

19. With regards to claim 47, Vogt fails to teach, but Dell teaches during the idle period, there are no transactions carried out by the memory controller on the memory bus that involve the storage array (column 2, lines 8-35, and column 3, lines 23-64). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the idle error correction system of Dell with the memory buffering error correction units Vogt of in order to decrease the number of errors without lowering system efficiency.

20. With regards to claim 48, Vogt teaches checking bus errors in transactions across the memory bus between the memory controller and the memory device, by a bus error logic of the memory device (paragraph 83); but fails to teach requesting the memory controller to retransmit the read command if the bus errors are detected. However, official notice is here given that the requesting of retransmission of data in response to errors being detected is notoriously well known in the art at the time of invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to well known retransmission requests on discovery of an

error with the memory buffering error correction units Vogt of in order to decrease the number of propagated errors without lowering system efficiency.

21. Claims 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,845,472 to Walker et al. in further view of U.S. Patent Application Publication 2002/0167791 to Goris.

22. With regards to claim 42, Walker does not teach the interfaces using a point-to-point topology. Goris teaches the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface, a second interface, a second memory bus coupled to the second interface (Fig. 7, paragraphs 23-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker using the point to point topology of Goris in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

23. With regards to claim 43, Walker teaches a first memory bus coupled to the memory controller (column 3, line 63, through column 4, line 11), but does not teach the interfaces using a point-to-point topology. Goris teaches the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface, a second interface, a second memory bus coupled to the second interface; and a second memory device having a second storage array comprised of a plurality of memory cells and a second interface buffer coupled within the second memory device to the second storage array, wherein the second interface buffer provides a third interface by which the second memory device is coupled to the second

memory bus forming a point-to-point connection between the third interface and the second interface, (Fig. 7, paragraphs 23-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker using the point to point topology of Goris in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

24. With regards to claim 44, Walker teaches during the idle period, there are no transactions carried out by the memory controller on the first memory bus that involve the first storage array (column 8, lines 46-51).

25. With regards to claim 45, Goris fails to teach that each of the point-to-point memory interfaces contains error logic. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker in each interface of the point to point topology of Goris in order to take advantage of the speed increases of distributed resources in point to point topologies over arbitrated topologies.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D. Schneider whose telephone number is (571) 272-4158. The examiner can normally be reached on M, T, Th, and F, 9-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDS

KIM HUYNH
SUPERVISORY PATENT EXAMINER
7/6/07